

Technical Notes on using Analog Devices' DSP components and development tools

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Setting Mode Pins on Reset

Q:

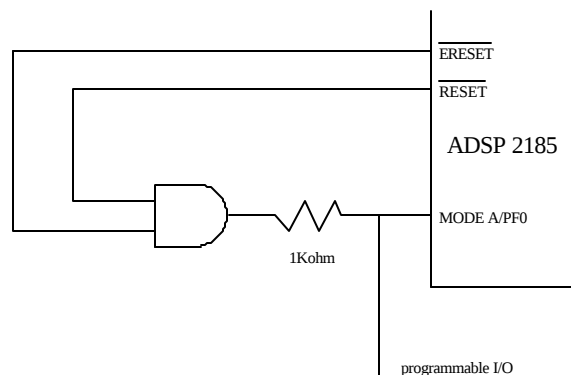
Hi, I'm developing a DSP system using an ADSP-2185 (100 pin package). The design requires me to use the Programmable Flag pins during program execution, which I noticed are multiplexed with the Mode A, B and C pins. I am concerned that there may be problems in latching the proper setting on the Mode pins when a RESET is asserted. I also understand that there are concerns when using an EZ-ICE to simulate a design which involves a 100 pin package. Can you suggest some general guidelines for designing a system which latches mode information correctly for both general execution and system emulation?

A:

On all ADSP-218x parts which are packaged in a 100-pin Thin Quad Flat Pack (TQFP), some of the pins are multiplexed to retain all of the functionality of the larger packaged ADSP-218x DSPs. In particular, the DSP can be booted in either BDMA or IDMA mode by properly setting the Mode C pin. The DSP cannot change modes while in operation; this information is only latched on a reset. Once booting has been initiated, the Mode C pin is used as a programmable flag (PF2). If you are using the mode pins in your design, care must be taken at reset to set them properly. Also, when you are using the EZ-ICE to emulate a design, it is important to remember that the ERESET pin acts exactly like RESET. This means that mode information is also latched on an emulator reset as

well as a chip reset. This could force a slight modification in your system to create an emulator compliant design.

There are two methods of setting the Mode pins on reset: static and dynamic. A static mode selector would involve either a pull up or pull down resistor tied to each mode pin. A resistor value of 10k Ω is recommended to minimize power dissipation and to ensure correct biasing of the input. In a dynamic mode configuration, the mode pins must be connected to a logic gate driven by RESET and ERESET (only RESET is necessary if you are not emulating your design). As an example, if you wanted to set Mode A to zero on a reset or emulator reset, the following wiring could be used:



This circuit will drive the Mode A pin properly and also allow it be used as a programmable flag pin when the DSP is in normal operation.

Clocking the DSP During Reset?

Q:

In my ADSP-2181 design, I am investigating different options to minimize power consumption. Can you tell me when it is necessary to supply a CLKIN signal to the DSP and when it would be possible to turn off this input?

A:

On all ADSP-21xx (and ADSP-21xxx) DSPs, it is necessary to supply a CLKIN signal when RESET is first asserted. This input is used to set initial internal register values in the DSP. If a clock is not supplied, the transistors could be forced into an unknown state and numerous problems might occur. Once the DSP has been supplied a CLKIN signal for approximately twelve cycles, the registers will have reached a stable state, and the clock signal can be removed. Before exiting the reset state (de-assertion of RESET), it is necessary to supply the DSP with a clock for at least 2000 cycles to give the phase-locked loop (PLL) adequate time to synchronize system clocks before